**Lecture #19 Worksheet, Answer Master**

**Fill in blanks to answer questions below. Then email this sheet to your TA.**

1. **What it the purpose of the MIPS control unit?**

   **The control unit decodes instructions to determine CPU operations.**

2. **What two bit-fields (i.e., group of bits) of the instruction go directly into the CPU? What are the names of the two bit-fields?**

   **Bits 0-5 are the op code ("operation code"), which determines the type of instruction. Bits 26-31 contain the function code, which tells the CPU what kind of register-to-register instruction is selected (when the op code = 0).**

3. **What three bit-fields go directly to the register block, and what physical hardware do they designate?**

   **The three fields that identify registers in the instruction go to the register block. The first (left-most) field identifies the destination register, where the result of a register-to-register instruction is stored. The second field is the first source register (Rs), containing one of the operands to be processed. The third field (right-most) contains the second operand in the instruction.**

4. **What six-bit field does the ALU control use?**

   **The ALU control hardware uses the function code field (bits 0-5) to determine**

**the type of instruction for register-register instructions.**

5. **The diagram on slide 7 shows that only three bits, for a total of 8 possible operations, are sent to the ALU, even though the ALU control block has eight inputs, which could be used to identify up to 256 ALU functions. Why are so many inputs used but so few possibilities included?**

   **The ALU Control Block was designed with the possibilities of future upgrades in mind.**

6. **The Control Decoder decodes what bit field?**

   **The op code field.**

7. **What does the Mem-to-Reg control line select?**

   **It selects whether the result of an ALU operation or a data retrieval from memory is written back to the register block.**

8. **What do the Mem Read and Mem Write lines do?**

   **They tell the CPU if data is to be stored to or retrieved from memory.**

9. **What does the ALU Source line do?**

   **It selects whether the contents of the Rt register or the sign-extended immediate is sent to one of the ALU inputs in an operation.**

10. **Study the value of the op code control signals (that is, 0 or 1), and what each value signifies to the ALU (slides 9 and 10).**

11. **Study the op code decoder diagram shown, and understand how different**

**instructions can activate the same control line.**

12. **As a register-to-register instruction is processed (slides 14-17), how many control lines are activated? Count the two lines from the Op Code decoder to the ALU Control decoder as a single line.**

    **Five "control lines" are activated—the ALU Control line, the ALU Source line, the ALU op line, the Reg Write line, and the Mem/Select line.**

13. **With the same assumptions as in Question 12, how many lines are activated?**

    **Six. The five noted above, plus the Mem Write line.**

14. **With the same assumptions as in 12 and 13, how many control lines are activated in a branch instruction?**

    **Only four—the ALU Op, the ALU Control, the Branch activated bit, and the branch MUX Control lines.**

15. **When adding the jump control circuitry, how many MUX's are included in the CPU design?**

    **Five—the register block write select, the ALU input select, the Memory or ALU result select, the branch select, and the jump select.**

16. **With the signal and data paths in an active jump instruction, how fast do you think that the jump is executed?**

    **Very fast. It does not involve an ALU operation, memory access, or register block access.**

**17. Complete exercise 1 and then check your answers on slide 24.**

**18. Explain the inefficiency of the single-cycle architecture (slides 25 and 26).**

**The single-cycle architecture allows one instruction every clock cycle. But that means that it must be long enough to allow completion of a load from memory cycle, which is the longest instruction. But most instruction take less time. That means that in allowing the time in a cycle to complete a load instruction, significant time is wasted in each cycle for other instructions.**

**19. Explain the multicycle implementation approach.**

**In the multicycle implementation, each instruction is divided into five parts, and the clock runs five times as fast. Since most instructions do not use all five parts of the instruction (see slides 29 and 30), those time-consuming parts may be skipped for instructions that do not need them, saving substantial time.**

**20. What is the speed advantage for the multicycle implementation?**

**It is 30%+.**

**21. What else is saved?**

**The multicycle approach also saves some hardware costs.**

**22. One problem with the multicycle implementation is that during each clock cycle, only one-fifth of an instruction is completed—it takes 5 clock cycles to complete one instruction. Thus, partial results after each cycle before the last one must be preserved. Referring to slides 33 and 34, what data must be**

**saved?**

**The four data sets that must be preserved are (1) the 32-bit instruction, (2) the 32-bit contents of the Rs and Rt registers, (3) the results of the ALU operation, and (4) the data from memory during a read operation.**

**23. From slide 35, what new operations does the ALU have to perform?**

**It updates the program counter and also calculates branch addresses.**

**24. Slide 37 shows the full multicycle implementation CPU, with all control functions included. Name any three of the new control lines that are added (above those on the single cycle CPU).**

**The PC Write line, the PC Write Condition line, the Instruction/Data Read line, the ALU Source A and B lines (was just one ALU source line before), the Instruction Register Write line, and the Program Control Source Write line.**

**25. Although students do NOT need to memorize this CPU variant for the final test, they should study it so that the transition to the pipeline architecture will be more understandable.**

**26. Do Exercise 2 on slide 39 (use the diagram on slide 40), then check your answers on slide 41.**